

# III

## Operational Amplifiers

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### Chapter 1

The operational amplifier, so named for its early association with precision computing networks to simulate various mathematical *operations*, is truly a workhorse in A-D conversion and interface circuits, as well as in general Electronics. Its applications include scaling and input conditioning, sample-hold, precision comparisons, current-to-voltage conversion and voltage-to-current conversion, active filters, etc.

For a broad understanding of the operational amplifier and a panoramic view of its possibilities, the reader is referred to any of the (many) papers, handbooks, and textbooks now in print. The objective of this chapter is to assist the reader in selecting the best operational amplifier for the job. But we start with a brief discussion of “op amp” principles, followed by a guide to definitions and specifications.

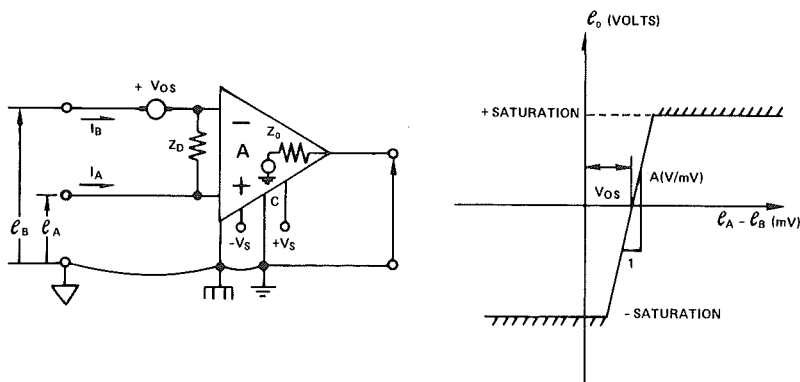
### UNDERSTANDING OPERATIONAL AMPLIFIERS

While there is no single commercially-available op amp that can meet the requirements of every application (the *ideal op amp*), the concept of an ideal operational amplifier is helpful in the initial analysis of a given configuration, and for synthesizing basic circuit configurations to perform given mathematically-described tasks. In short, the ideal device is useful for deriving closed-loop relationships that can be directly applied to real circuits, with little error in many cases. When the desired circuit configuration has thus been established, it is not difficult to analyze error in terms of

*statics* (dc offset errors) and dynamics (gain, common-mode errors, and response to rapidly-changing inputs), to determine the required amplifier parameters.

### *The Ideal Op Amp*

The accepted symbol\* for an operational amplifier is shown in Figure 1. The triangle points in the direction of causal signal flow. Considering the amplifier as a four-terminal network, the output,  $e_o$ , is related to the inputs ( $e_A - e_B$ ) as shown graphically in Figure 1. For changes in  $e_A$  that are positive with respect to  $e_B$ , the output moves in the same sense (or phase), and the terminal at  $e_A$  is therefore marked “+” for *non-inverting*, or *reference* input. Since corresponding variations in  $e_B$  cause the output to move in the opposite sense (or  $180^\circ$  out-of-phase), this terminal is marked “-” for *inverting* input. The “-” input is frequently called the *summing point*, for reasons that should shortly become clear.



*Figure 1. Operational Amplifier — Block Diagram and Response*

\*Some use a triangle with a curved back, the vestige of a practice sporadically employed in the analog computing field to distinguish open-loop amplifiers from committed amplifiers. However, since the first major publication devoted to operational amplifiers as circuit elements, the “GAP/R Applications Manual,” appeared in 1956, the straight-backed triangle has been the symbol of choice.

Although the negative input is conventionally drawn above the positive input, it is often convenient, when sketching circuits, to interchange their locations. This is permissible, if they are appropriately, clearly, and unambiguously marked (and the circuit is drawn correctly).

The idealized properties generally assumed for deriving the ideal performance of circuits employing the amplifier of Figure 1 are:

Open-loop gain	$A \rightarrow \infty$ dc to high frequencies	typical value: 100kV/V
Voltage offset	$V_{os} = 0$ volts	typical value: $\pm 1\text{mV}$ @ $25^\circ\text{C}$
Bias currents	$I_A = I_B = I_b = 0$ amperes	typical values: $10^{-14}$ to $10^{-6}$ A
Input impedance	$Z_D \rightarrow \infty \Omega$	typical values: $10^5 \Omega$ , $10^{11} \Omega$
Output impedance	$Z_o = 0$ ohms	typical values: 1 to $10 \Omega$
Common-mode rejection	CMRR $\rightarrow \infty$	typical values: 60dB to 120dB

From the ideal considerations noted above, it is evident that the op amp will act much like a two-level high-gain comparator if used open-loop. In fact, comparators are essentially op amps in which open-loop speed has been optimized at the expense of closed-loop stability. To achieve the many benefits of operational circuitry, though, it is necessary to employ negative feedback. With negative feedback, the operational-amplifier circuit is in effect a control loop dedicated to maintaining the "error" voltage between the inputs equal to zero. In fact, if the output voltage is to be within its linear range,  $e_A - e_B$  must approach zero.

$$e_A - e_B = \frac{e_o}{A} \quad (1)$$

As

$$A \rightarrow \infty, e_A - e_B \rightarrow 0$$

or,

$$e_A \cong e_B \quad (2)$$

\*Dynamic summing-point error is often written as

$$e_A - e_B = \frac{e_o}{A} + \frac{e_A}{\text{CMRR}}$$

or the instantaneous (or vector) sum of differential gain error and common-mode error. Although common-mode voltage would be conventionally defined as  $(e_A + e_B)/2$ , difficulties stemming from the use of  $e_A$  alone tend to be negligible, because  $e_A$  and  $e_B$  are usually very-nearly equal.



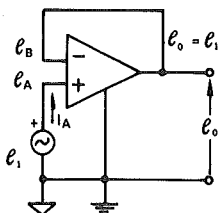
For example, in order for  $e_o = 8V$ , if  $A = 100,000$ ,  $e_A - e_B = 80\mu V$ .

The simplest feedback circuit that one might devise is the ideal unity-gain follower of Figure 2, in which 100% of the output voltage is fed back to the negative input. The input signal source is connected directly to the non-inverting input, and the output follows precisely. Summing voltage around the loop,

$$e_1 + (e_B - e_A) - e_o = 0 \quad (3)$$

since

$$e_B - e_A \rightarrow 0, e_o = e_1 \quad (4)$$



**Figure 2. Unity-Gain Follower**

The gain is precisely unity. The input impedance is infinite, and the output impedance is zero, because we are considering an ideal amplifier. For practical applications, the major factors limiting performance of this circuit are the common-mode voltage range and error, as well as bias current (if source impedance is high). Changes of bias current with common-mode level may also be important, since many manufacturers specify it at zero common-mode voltage only.

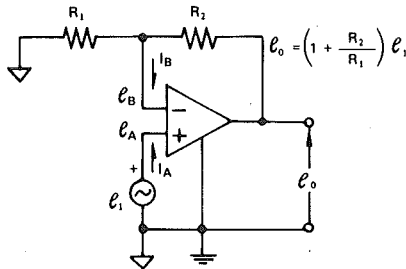
## *Non-Inverting Amplifier*

In Figure 3, instead of feeding back the entire output voltage, it is divided down through a simple attenuator, to reduce the feedback voltage. Thus,

$$e_1 + (e_B - e_A) - \frac{R_1}{R_1 + R_2} e_o = 0 \quad (5)$$

and

$$e_o = \left[ \frac{R_2}{R_1} + 1 \right] e_1 \quad (6)$$



*Figure 3. Non Inverting Amplifier*

The gain is ideally determined solely by the passive components used, is positive, and must be equal to or greater than unity. Note that the voltage follower is simply the special case for  $R_2 = 0$ . Again, input impedance is infinite for  $I_A = 0$ , and output impedance is zero. However,  $R_2 + R_1$  are now part of the load on the op amp output. The same basic limitations as for the follower apply, except that the magnitude of the common-mode problem is generally reduced as the required gain is increased, since the maximum non-saturating input is determined by the ratio of maximum output to maximum input.

### *Inverting Amplifier*

The basic circuit for the inverting amplifier is shown in Figure 4. In this case, the non-inverting, or reference input is connected directly to signal/power ground, and the input signal is connected at  $R_1$ , which forms part of the negative-feedback network. Unlike the non-inverting case, where  $e_B$  follows the input signal  $e_A$



through a common-mode range,  $e_B$  (still following  $e_A$ ) is constrained to zero, within the gain error of the amplifier (i.e.,  $e_o/A$ ). That is,  $e_B$  will behave as a *virtual ground*.

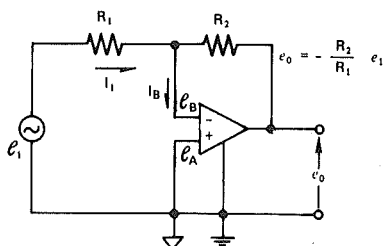


Figure 4. Inverting Amplifier-Attenuator

The analysis is quite straightforward: summing currents at B,

$$\frac{e_1 - e_B}{R_1} + \frac{e_o - e_B}{R_2} - I_B = 0 \quad (7)$$

Since

$$e_B = e_A = 0, \text{ and } I_B = 0,$$

$$\frac{e_1}{R_1} + \frac{e_o}{R_2} = 0 \quad (8)$$

and

$$e_o = - \frac{R_2}{R_1} e_1 \quad (9)$$

Again, the gain is determined solely by the passive components used to set the amount of feedback, but this time the output is an inverted version of the input. Input impedance seen by the signal source is now  $R_1$ , while output impedance remains zero.

There are a number of useful properties inherent in this circuit:

1. *Virtual ground.* Voltage  $e_B$  is essentially at ground potential.

2. *Voltage-to-current transconductance.* The current through  $R_2 (= e_o/R_2)$  is determined by  $e_1/R_1$ , independently of  $R_2$ .  $e_o$  becomes whatever voltage is necessary (within limits) to maintain

the current  $e_1/R_1$ . This is true irrespective of the nature of the element labeled  $R_2$ , which may be nonlinear (e.g., a diode), or contain storage (e.g., be a capacitor, in which case  $e_o = -(1/RC) \int e_1 dt$ ), or be an  $n$ -terminal network (e.g., an attenuator).

3. *Current-to-voltage transresistance.* If a current source  $i$  is connected at B, the current will flow through  $R_2$  to the output, and develop an output voltage  $-iR_2$ , which depends only on the values of  $i$  and  $R_2$ . The virtual ground at B is an ideal load for a current source. Output resistance is reduced by the *loop gain* (p. III-8).

4. *Summation.* Since the terminal B must be maintained at virtual ground, any number of currents developed by current sources, voltages-and-resistors, etc., may be independently applied, and their algebraic sum will flow through  $R_2$ , developing an output voltage  $-e_o = \sum i_{IN} R_2$  (Figure 5).

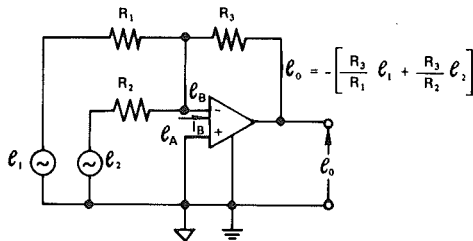


Figure 5. Inverting Summing Amplifier

There are a few additional comments that may be made about this circuit, since misunderstandings often develop:

1. The summing point (B) behaves as a virtual ground, or current sink *only while the amplifier's behavior is linear*. If the amplifier's output voltage or rate-of-change of output is in limits, it is no longer amplifying and must be treated in terms of an equivalent circuit appropriate to its new mode of operation.

2. In normal operation, since there is little voltage difference across the differential input, the impedance,  $Z_D$ , has negligible effect on the circuit behavior.  $R_1$  is the input impedance



presented to  $e_1$ . For computations,  $R_1$  includes the input signal's source impedance.

3. If the amplifier is used in a charge mode (e.g., with  $R_1$  or  $R_2$ , or both, replaced by capacitance, to form a differentiator, integrator, or charge amplifier) it is often desirable to maintain resistance in series with the amplifier's input terminal to protect it against transient charging currents, especially in high-voltage charge-amplifier applications.

### *Gain, Errors, and Stability*

There are five kinds of "gain" defined for operational-amplifier circuits:

*Open-loop gain* ( $A$ ) is the relationship, previously defined, between the output voltage\* and the differential input voltage.

*Feedback ratio* ( $\beta$ ) is the net amount of voltage fed back from the output to the amplifier's input. It is a function of the entire circuit from output back to input, including both designed and stray circuit elements and the input-impedance characteristics of the amplifier. Its inverse ( $1/\beta$ ) is often called the *closed-loop gain*, or "noise" gain; in fact, it is the *ideal* closed-loop gain.

*Loop gain* ( $A\beta$ ) is the fraction of open-loop gain that is available for error-correction. Its magnitude is a figure-of-merit for a particular circuit configuration. Its magnitude/phase relationship can be used to predict circuit stability.

*Closed-loop gain* is the gain for signals in series with the positive input (or, with opposite polarity, for a signal directly in series with the negative input). Closed-loop gain is

$$\frac{1}{\beta} \cdot \left[ \frac{1}{1 + \frac{1}{A\beta}} \right] \quad (10)$$

\*with a specified value of load resistance. Lighter loading usually results in somewhat higher open-loop gain, depending on the output impedance. It is generally preferable, as well as realistic, to specify loaded gain rather than unloaded gain (with an output-resistance calculation), since load can be more-easily increased (if necessary) than decreased.



Since offset voltage, drift, and noise voltage are specified as “referred to the input,” they are amplified by this term. For this reason, it is also called the “noise” gain. For  $A\beta \gg 1$ , closed-loop gain is  $1/\beta$ .

*Signal gain* is the closed-loop transfer relationship between the output and any signal-input to an operational-amplifier circuit. For example, if the amplifier is connected as an inverting summing amplifier with gains of 1 and 3 for the two inputs being summed,  $\beta = 1/5$ ; closed-loop gain is approximately 5;  $A\beta$  (for  $A = 100,000$ ) is 20,000; and a  $100\mu\text{V}$  offset, referred to the amplifier’s input, becomes  $0.5\text{mV}$  at the output. Referred to the *actual* signal inputs, the offset is  $0.5\text{mV}$  (gain-of-1), and  $167\mu\text{V}$  (gain of 3).

## Difference Amplifier

There is no universally-applicable approach to analyzing op amps connected differentially. However, the equivalent circuit of Figure 6 probably represents one of the most useful configurations.

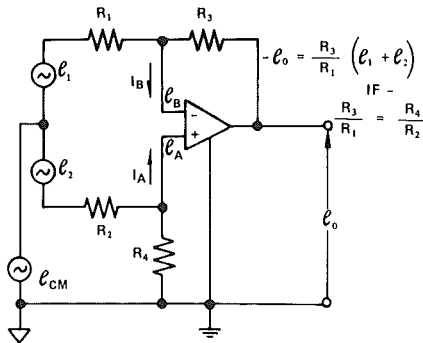


Figure 6. Difference Amplifier Configuration

If  $e_{\text{CM}}$  is zero, the circuit is the familiar subtractor, while, for  $e_1$  or  $e_2$  zero, the circuit reduces to a simple bridge or differential amplifier, with or without the common-mode voltage  $e_{\text{CM}}$ . Using the known results derived earlier for the non-inverting and inverting cases, and the theorem of superposition, and with the usual assumptions for ideal behavior,

$$e_o = -e_1 \frac{R_3}{R_1} + e_A \left[ 1 + \frac{R_3}{R_1} \right] - e_{CM} \frac{R_3}{R_1} \quad (11)$$

Since

$$\begin{aligned} e_A &= e_2 \frac{R_4}{R_2 + R_4} + e_{CM} \frac{R_4}{R_2 + R_4} \\ &= e_2 \frac{R_4}{R_2} \left[ \frac{1}{1 + \frac{R_4}{R_2}} \right] + e_{CM} \left[ \frac{R_4}{R_2} \frac{1}{1 + \frac{R_4}{R_2}} \right] \quad (12) \end{aligned}$$

$$e_o = -e_1 \frac{R_3}{R_1} + e_2 \frac{R_4}{R_2} \left[ \frac{\frac{R_3}{R_1} + 1}{\frac{R_4}{R_2} + 1} \right] + e_{CM} \left[ \frac{R_4}{R_2} \cdot \frac{\frac{R_3}{R_1} + 1}{\frac{R_4}{R_2} + 1} \right] - \frac{R_3}{R_1} \quad (13)$$

If

$$\frac{R_4}{R_2} = \frac{R_3}{R_1}$$

then

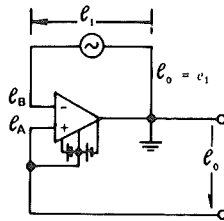
$$e_o = (e_2 - e_1) \frac{R_3}{R_1} \quad (14)$$

It is (obviously) important to ensure that  $R_3/R_1 = R_4/R_2$ , if common-mode errors due to  $e_{CM}$  are to be eliminated.  $R_1$  and  $R_2$  should include the internal impedances of the sources  $e_1$  and  $e_2$ . The source impedance of  $e_{CM}$  is of importance only to determine the actual amount of common-mode signal level at  $e_A$ . The actual common-mode signal seen by the *amplifier* is  $e_A$ , not  $e_{CM}$ .

Any common-mode error in the above expression is due to resistance-ratio mismatch. The common-mode response of the amplifier itself will increase or decrease that number. If the circuit is linear, the introduction of a small mismatch in resistor ratio may be used to compensate for the amplifier's common-mode error, in many cases.

*Inside-Out Follower*

As mentioned earlier, the op amp is a 4-terminal device, although one or more terminals may be restricted in use (e.g., the chopper-stabilized amplifier). To achieve follower operation with a single-ended chopper-stabilized amplifier, it is usually necessary to "float" the power supply, as shown in Figure 7. Negative feedback is derived from power common to the non-inverting input; then,  $e_o = e_1$ .



*Figure 7. "Inside-Out" Follower*

One benefit of this circuit (also applicable to bipolar differential amplifiers) is its ultra-high input impedance, since the common-mode impedance is now bootstrapped by the power-supply isolation impedance. However, cost is not trivial, since the amplifier requires a separate supply.

*Summary of "Understanding Operational Amplifiers"*

Each of the circuits described in this section has been developed with resistive feedback elements. In general, any complex linear or nonlinear feedback element, passive or active, may be used (if the configuration is stable) with appropriate modifications of the analysis to include the reactive or nonlinear relationships.

Typical applications include voltage-to-current and current-to-voltage conversion, sums and differences, scaling, rectifying, filtering, modulating, demodulating, classifying, peak-following, log(arithm)ing, multiplying/dividing/rooting, integrating, differen-



tiating, oscillating, phase shifting, bridging, push-pulling, etc. The number of possible useful circuits using op amps staggers the imagination.

In sum, the power of the feedback technique resides in the gain that is so high that performance of the circuit depends, not on the open-loop gain of the amplifier, but on the external components and the configuration in which they are connected.

The equation that determines viability of a given circuit from the dynamic point of view is

$$e_o = \frac{\text{Ideal Relationship } f(e_1, e_2, \dots e_n)}{1 + \frac{1}{A \cdot \beta}} \quad (15)$$

The magnitude of  $A\beta$  determines functional fidelity, and its phase relationship, following the requirements of Nyquist and Bode, the circuit's stability (the total phase shift must be less than  $180^\circ$  at the highest frequency at which  $|A\beta| \geq 1$ .)

### *Static Errors of Op Amps*

In deriving the idealized (yet practical) circuits described above, it was assumed that the amplifier possessed ideal properties. It is of course the departures from the ideal that determine the specifications of the amplifier and its properties in a given application. We have already touched on some dynamic specifications (gain and CMRR), and hinted at those that affect response and stability. In this section, we shall touch on those that affect steady-state precision.

In Figure 8, there appear an equivalent voltage offset  $V_{os}$  (which could be in series with either input) and bias-current errors,  $I_A$  and  $I_B$  at each input, respectively. Since other input impedances may contribute non-negligible error, they are lumped in with  $R_3$  and  $R_4$ . Summing input currents at B,

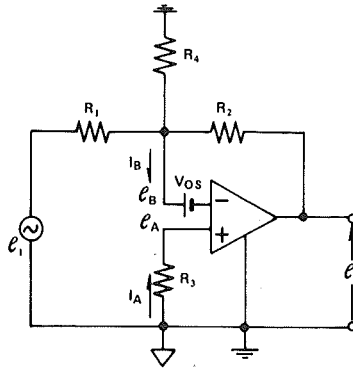


Figure 8. Voltage and Current Offset Errors

$$0 = \frac{e_1 - e_B}{R_1} + \frac{e_o - e_B}{R_2} - \frac{e_B}{R_4} - I_B \quad (16)$$

or

$$e_o = -e_1 \frac{R_2}{R_1} + e_B \underbrace{\left[ 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right]}_{\epsilon_{RTO}} + I_B R_2 \quad (17)$$

$$\epsilon_{RTO} = (e_B + I_B R) \left[ 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right]$$

where

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_4} \quad (18)$$

Now,

$$e_B = e_A + V_{os} = -I_A R_3 + V_{os} \quad (19)$$

Thus,

$$\epsilon_{RTO} = (V_{os} + I_B R - I_A R_3) \left[ 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right] \quad (20)$$

If  $R_3 = 0$ ,

$$\epsilon_{RTO} = (V_{os} + I_B R) \left[ 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right] \quad (21)$$

If  $R_3 = R$ , (i.e.,  $\frac{1}{R_3} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_4}$ )

$$\epsilon_{RTO} = (V_{os} + \{I_B - I_A\} R) \left[ 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right] \quad (22)$$

From equations (21) and (22), it is evident that errors attributable to bias currents  $I_A$  and  $I_B$  can be equated to an equivalent offset voltage at the summing point  $(I_A R_3 - I_B R)$ . If  $I_A = I_B$ , then by selecting a resistor  $R_3$ , equal to  $R$ , bias-current error can be reduced to that of offset or difference current,  $(I_B - I_A)R$ . This technique is often useful, but it is important to note that it can be downright detrimental with some amplifier configurations. It works best with bipolar transistor input designs, as offset is generally an order of magnitude smaller than bias currents, and bias current errors generally are large enough so that "any" change is an improvement. However,  $R_3$  is less effective, and questionable, with FET-input op amps, where offset current can equal bias current, and it is harmful with chopper-stabilized or varactor-bridge designs. Also, it is ineffective or impractical in circuits having complicated circuitry in which resistances (e.g., potentiometer settings) can change, circuits are switched, or capacitors play a major role (e.g., integrators), since any changes on one side must be imaged on the other.

## CHOOSING AN OP AMP

Selecting the best amplifier for a particular application has become almost an art when you consider the overwhelming proliferation of both integrated-circuit and modular devices. On the other hand,

the choice has become somewhat easier at Analog Devices, because both IC and modular devices are available, including some that are unique in the industry. Having a wide repertoire available, our applications engineers (and customers) benefit by the possibility of a truly disinterested choice, based not on what one has to sell, but on the needs that must be fulfilled.

The following sections are intended to guide the user to the best choice for his application, whether he be expert or newcomer. Familiarity with amplifier types and specifications naturally tend to facilitate the choice.

First there will be a discussion of the classification of amplifiers, with a table illustrating the specifications of representative devices in the various classes. Then there is a listing of the definitions of specifications. For an excellent and thorough (but too lengthy to include in this volume) discussion of selection principles for operational amplifiers, we strongly urge the reader to consult the *Analog Devices Product Guide, 1972*, or, if out of print, its successor publications.

## CLASSIFICATION OF AMPLIFIERS

Table 1, which appears on the next two pages, is a capsule selection guide, outlining the key parameters of a wide range of both IC and modular devices. They are divided into seven major classes, based on key application features:

Key Feature	Application	Amplifier Classification
Low drift and noise, long term stability	Medical and industrial, transducers, amplifiers, preamps	{ Low drift chopper { Low drift differential
Low bias current	High source impedance, integrators, charge amplifiers	{ General purpose FET { Electrometer
Wideband and fast settling	D/A, A/D converters, sample and holds, comparators	Wide bandwidth fast settling
Economy, moderate performance	Function generators, general designs, active filters	{ General purpose bipolar { General purpose FET
Voltage and/or current booster	Audio and servos, power regulators, galvanometers, current source	High output capability

**Table 1.**
**Capsule Selection Table:**

Description	Model	Open Loop Gain	Rated Output	
		V/V	V	mA
General Purpose — Bipolar				
Moderate Performance Op Amps				
Good Performance Economy	118 A/K	250k	±10	±5
Low Cost, 20mA Output	119 A/K	500k	±10	±20
Slew Rate, High Gain, IC	AD507 J/K	80k	±10	±10
Economy, Speed, IC	AD201A	50k	±10	±5
Lowest Cost, General Purpose, IC	AD741 K/L	50k	±10	±5
Super Beta-Low 2nA $I_{bias}$ IC	AD208/A	50k/80k	±13	±1.3
General Purpose FET —				
Low Bias Current, High $Z_{in}$ Op Amps				
Lowest Cost Discrete	40 J/K	50k	±10	±5
Guaranteed CMR — Low Bias	43J	50k	±10	±5
Lowest Bias — High CMR	41 J/K/L	100k	±10	±5
Lowest Drift — 20mA Output	146 J/K	100k	±10	±20
Best Choice — Economy IC	AD503 J/K	20k/50k	±10	±5
Hybrid — Lowest Offset & Bias, IC	AD511 A/B	25k	±10	±5
High GBW, Slew Rate, IC	AD513 J/K	20k/50k	±10	±5
Wide Bandwidth —				
Fast Settling Op Amps				
1000V/ $\mu$ s Slew, 100ns Settling, 100mA	46 J/K	25k	±10	±100
125V/ $\mu$ s, 250ns Settling to 0.1%	48 J/K	100k	±10	±20
Lowest Cost —1 $\mu$ s Settling to 0.01%	45 J/K	50k	±10	±20
0.01% Buffer, 1 $\mu$ s to 0.01%	44 J/K	100k	±10	±20
100MHz GBW, Lowest Drift	120 A/B	500k	±10	±25
Wideband, 130V/ $\mu$ s, IC	AD505 J/K	100k/250k	±10	±5
Low Voltage Drift —				
Chopper Stabilized Op Amps				
0.1 $\mu$ V/ $^{\circ}$ C Drift — Lowest Noise	234 J/K/L	10M	±10	±5
Lowest Cost — General Purpose	233 J/K/L	10M	±10	±5
Low Cost, Non-Inverting, High $Z_{in}$	260 J/K	5M	±10	±5
General Purpose — 25mA Output	231 J/K	10M	±10	±25
High Bandwidth — 20mA Output	210/211	100M	±10	±20
Low Voltage Drift —				
Differential Input, High CMR Op Amps				
Lowest Cost — 0.25 $\mu$ V/ $^{\circ}$ C	184 J/K/L	300k	±10	±5
Battery Powered — Gen. Purpose	153 J/K	50k	±1.0	±1.0
Lowest Bias, 4nA, 0.5 $\mu$ V/ $^{\circ}$ C	180 J/K	300k	±10	±2.5
Super Beta, 1 $\mu$ V/ $^{\circ}$ C, 20nA, IC	AD508 J/K/L	250k/500k/1M	±10	±5
Highest CMR, Low Offset and Drift, IC	AD504 J/K/L	250k/500k/1M	±10	±5
Electrometers —				
Ultra Low Bias Current				
Varactor, Inverting	310 J/K	100k	±10	±5
Varactor, Non-Inverting	311 J/K	100k	±10	±5
Lowest Cost — High Gain FET	42 J/K/L	300k	±10	±5
High CMR, Wideband	41 J/K/L	100k	±10	±5
FET, Input, IC	AD523 J/K/L	75k	±10	±5
High Output Voltage or Current Op Amps				
100mA Booster — Lowest Cost	B100	0.85	±10	±100
20V, 20mA Output — High CMR	163 A/K	500k	±20	±20
20 $\mu$ V, 5mA Output — Economy	165 A/K	250k	±20	±5
100mA Output — 10MHz $f_p$ — Diff Input	46 J/K	25k	±10	±100
Guaranteed 10mA vs. Temp, IC	AD512 K/S	50k	±12/±10	±12/±10

Based on Analog Devices, Inc. Product Guide — 1972



## Operational Amplifiers

Frequency Response			Offset Voltage vs. Temperature	Input Bias Current	
Unity Gain MHz	Full Power kHz	Slew Rate V/ $\mu$ s		@25°C	vs. Temperature
			$\mu$ V/°C max	pA	pA/°C
1.5	100	6.0	$\pm 20/\pm 5$	0, +35nA	$\pm 0.6/\pm 0.5$ nA/°C
1.5	100	6.0	$\pm 20/\pm 5$	0, +35nA	$\pm 0.6/\pm 0.5$ nA/°C
35	320	20	$\pm 15/\pm 15$ max	$\pm 25$ nA	—
1.0	10	0.5	$\pm 15$	$\pm 75$ nA	—
1.0	10	0.5	$\pm 15/\pm 5$	$\pm 75$ nA	—
1.0	10	0.3	$\pm 15/\pm 5$	$\pm 2.0$ nA	—
4.0	100	6.0	$\pm 50/\pm 20$	0, -50/-20	2x/10°C
4.0	100	6.0	$\pm 30$	0, -10	2x/10°C
1.0	50	3.0	$\pm 25/\pm 10/\pm 25$	0, -0.5/-0.25/-0.15	2x/10°C
5.0	150	10	$\pm 7/\pm 2$	0, -30/-20	2x/10°C
1.0	—	6.0	$\pm 75/\pm 25$	0, -15/-10	2x/10°C
1.0	70	5.0	$\pm 75/\pm 25$	0, -25/-10	2x/10°C
1.0	—	20	$\pm 75/\pm 25$	0, -30/-20	2x/10°C
40	10MHz	1000	$\pm 75/\pm 25$	0, -100	2x/10°C
15	1.5MHz (inv.)	125 (inv.)	$\pm 50/\pm 15$	0, -50/-25	2x/10°C
10	1MHz	75	$\pm 50/\pm 15$	0, -50/-25	2x/10°C
10	1MHz	75	$\pm 50/\pm 15$	0, -50/-25	2x/10°C
10-100	4MHz	250	$\pm 15/\pm 8$	0, +55nA	0.9/0.7nA/°C
10	2MHz	120	$\pm 15/\pm 8$ typ	$\pm 75/\pm 25$ nA	—
2.5	500	30	$\pm 1.0/\pm 0.3/\pm 0.1$	$\pm 100$	$\pm 4/\pm 2/\pm 2$
0.5	4.0	0.25	$\pm 1.0/\pm 0.3/\pm 0.1$	$\pm 50$	$\pm 2/\pm 1/\pm 0.5$
100Hz	2-50Hz	100V/sec	$\pm 0.3/\pm 0.1$	$\pm 300$	$\pm 10$
0.5	3.0	0.2	$\pm 0.25/\pm 0.1$	$\pm 100/\pm 50$	$\pm 1/\pm 0.5$
20	500	100	$\pm 0.5/\pm 1.0$	$\pm 100/\pm 150$	$\pm 1/\pm 3$
1.0	5.0	0.3	$\pm 1.5/\pm 0.5/\pm 0.25$	0, +25nA	$\pm 0.25$ nA/°C
0.15	5.0	0.02	$\pm 5.0/\pm 2.0$	$\pm 3$ nA	$\pm 0.1$ nA/°C
1.0	10	0.6	$\pm 1.5/\pm 0.5$	$\pm 4$ nA	$\pm 0.1/\pm 0.05$ nA/°C
0.3	1.5	0.12	$\pm 5.0/\pm 3.0/\pm 1.0$	$\pm 50/\pm 20/\pm 20$	—
0.3	1.5	0.12	$\pm 5.0/\pm 3.0/\pm 1.0$	$\pm 200/\pm 100/\pm 80$	—
2kHz	7Hz	0.4V/ms	$\pm 30/\pm 10$	$\pm 10$ fA	$\pm 1$ fA/°C
2kHz	7Hz	0.4V/ms	$\pm 30/\pm 10$	$\pm 10$ fA	$\pm 1$ fA/°C
1.0	4.0	0.25	$\pm 75/\pm 25/\pm 75$	0, -0.5/-0.25/-0.15	4(0 to +70°C)
1.0	50	3.0	$\pm 25/\pm 10/\pm 25$	0, -0.5/-0.25/-0.15	4(0 to +70°C)
0.5	70	5.0	$\pm 90/\pm 30/\pm 60$	-1.0/-0.5/-0.25	2x/10°C
—	1MHz	—	$\pm 1.0$ mV/°C	$\pm 500$ $\mu$ A	—
1.5	50	6.0	$\pm 20/\pm 5$	0, +35nA	$\pm 0.6/\pm 0.5$ nA/°C
1.5	50	6.0	$\pm 20/\pm 5$	0, +35nA	$\pm 0.6/\pm 0.5$ nA/°C
40	10MHz	1000	$\pm 75/\pm 25$	0, -100	2x/10°C
1.0	10	0.5	$\pm 20/\pm 25$	$\pm 200$ nA	—

(Specifications typical @ +25°C and rated power supply unless otherwise noted.)



Data for the table has been distilled from the *Analog Devices Product Guide — 1972*. It is suggested that the reader consult the latest *Product Guide* or supplement for information on the most-current product line. Copies of the *Guide*, as well as individual product data sheets, are available from Analog Devices or the nearest field office or representative.

In settling on the seven major classes, we have established what appears to be a near-optimum point of departure for proper amplifier selection. In some exceptional cases, an amplifier has been included in more than one category because of its outstanding versatility. But in most instances, one single attribute or key parameter is focussed on in each group. For example, the chopper-stabilized group naturally features low drift; however, it includes several models which could qualify for high output capability or wide bandwidth.

To ease the task of designers seeking the best device for a given job, based purely on its technical qualifications, both modules and IC's are listed together in each category. However, for the benefit of the many users who prefer IC's because of their low cost, small size, and hermetically-sealed package, we have clearly identified the IC members of each family as such under "Description."

## OPERATIONAL AMPLIFIER CLASSIFICATIONS

### 1. General Purpose — Moderate Performance

Amplifiers in this group include Analog's lowest cost devices. They are best suited for general purpose designs with moderate drift requirements in the range from 5 to  $40\mu\text{V}/^\circ\text{C}$ , unity gain-bandwidths to 1MHz, and full-power response to 100kHz. Typical applications include summing, inverting, impedance buffering (followers) and active filtering. They are also useful for developing nonlinear transfer functions.

### 2. General Purpose FET — Low Bias Current, High $Z_{\text{IN}}$

These models should meet most design requirements, especially those which cannot be satisfied by bipolar input designs because of excessive bias currents or too-low input impedance. The lower bias currents (0.15 to 100pA) and higher input impedances ( $10^{11}$  ohms) of FET's make them a natural choice when resistance values exceed 100k $\Omega$  and it is necessary to minimize input loading and current-offset errors to improve accuracy. Significant applications include integrators, sample and hold amplifiers, current to voltage converters and low-bias-current log circuits.

### 3. Wide Bandwidth — Fast Settling

Amplifiers in this group feature both differential FET and bipolar input stages, which afford a wide choice of drift and bias current specifications. They emphasize exceptionally fast response and wide bandwidths (to 40MHz, 100ns settling) for applications in data-acquisition and pulse-data transmission systems. Critical specifications are step response settling time, full power response and current output.

These amplifiers are useful for sample and hold circuits, A/D converters, and as high-speed buffers and integrators. Offering high output current capability, they should be considered for video or line driver circuits, D/A output amplifiers or as deflection coil amplifiers.



### *4. Low Voltage Drift – Chopper Stabilized*

These amplifiers are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve bandwidths to 20MHz, drifts to  $0.1\mu\text{V}/^\circ\text{C}$  and long term stability of  $2\mu\text{V}/\text{month}$ . Typical applications include error-summing amplifiers for servo loops, precision regulators, or as input amplifiers for laboratory grade metering instruments and test equipment.

### *5. Low Voltage Drift – Differential Input, High CMRR*

“Chopperless” low drift designs with differential inputs should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators and for impedance buffer designs. In general, they should be selected over single ended choppers where a differential input is required or whenever possible chopper modulation spikes are objectionable in the circuit design.

Amplifiers in this group feature differential bipolar transistor input stages achieving input drifts as low as  $0.25\mu\text{V}/^\circ\text{C}$ , offset voltages to  $100\mu\text{V}$  and exceptionally stable long term drifts of  $3\mu\text{V}/\text{month}$ . These devices offer differential performance with input noise of  $1\mu\text{V}$  p-p, a CMV of 10V and 100dB of CMR. For comparison, chopper-amplifier stability approaches  $1\mu\text{V}/\text{month}$ , but they are useful as single-ended amplifiers only.

### *6. Electrometer – Ultra Low Bias Current*

Amplifiers with bias currents less than 1pA are classified as suitable for electrometer use. Frequency response and voltage drift are usually secondary requirements. Both varactor bridge and FET-input designs are employed to achieve low bias currents, ranging from one picoamp ( $10^{-12}\text{A}$ ) to ten femtoamps ( $10^{-14}\text{A}$ ). These amplifiers are used as current-to-voltage converters with high impedance transducers such as photomultiplier tubes, flame detectors, pH cells and radiation detectors.

## 7. High Output – Voltage/Current

Amplifiers offered here have bipolar or FET inputs with output voltage swings of  $\pm 20$  volts or output current to  $\pm 100\text{mA}$ . Also included is model B100, a  $100\text{mA}$  wideband booster for op amps. Typical applications include audio amplifiers, voltage or current regulators and driver stages for sonar transducers, galvanometers and deflection coils.

## DEFINITIONS OF OP AMP SPECIFICATIONS

### *Absolute Maximum Differential*

Under most operating conditions, feedback maintains the error voltage between inputs very close to zero volts. However, in some applications, such as voltage comparators, the voltage between inputs can become large.  $E_d$  defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

### *Common Mode Rejection*

An ideal operational amplifier responds only to the difference voltage between inputs ( $e+$  minus  $e-$ ) and produces no output for a common mode voltage, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely subtracted at the output. If the output error voltage is referred to the input (dividing by closed loop gain) it reflects the common mode error voltage between the inputs. Common mode rejection ratio (CMRR) is defined as the ratio of common mode voltage to common mode error voltage. CMRR is sometimes expressed in dB.

$$\text{CMR} = 20 \log_{10} (\text{CMRR})$$

Precisely specifying CMRR is complicated by the fact that common mode voltage error,  $e_{cem}$ , can be a highly non-linear function of common mode voltage, and it also varies with temperature. This is particularly true for FET-input amplifiers. As a consequence, CMRR data published by Analog Devices are average figures assuming an end point measurement at the common mode voltage specified. The incremental CMRR about some large common mode voltage may be less than the average CMRR which is specified, but much greater at lower voltages. Published CMRR specifications apply only to DC input signals. CMRR decreases with increasing frequency.

### *Drift vs. Supply*

Offset voltage, bias current and difference current change with time as components age. It is important to realize that the published time drift for amplifiers does not accumulate linearly. For example, voltage drift for a chopper stabilized amplifier (which is by far the best amplifier type for long term stability) might be quoted as  $1\mu\text{V}/\text{day}$  whereas cumulative drift over 30 days would not exceed  $5\mu\text{V}$  nor  $15\mu\text{V}$  in a year. In general the drift accumulation may be extrapolated by multiplying the specified drift/day by the square root of the number of days. Since our catalog specifies drift/month, divide by  $\sqrt{30}$  or 5.5 to obtain drift/day.

### *Full-Power Response*

The large signal and small signal response characteristics of operational amplifiers differ substantially. An amplifier will not respond to large signal changes as fast as the small-signal-bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. We specify full power response in two ways: Full linear response and full peak response.

Full linear response,  $f_p$ , is the maximum frequency at unity closed loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. Note that this specification does not relate to "response" in the sense of gain reduction with frequency but

refers only to distortion in the output signal. There is no industry-wide accepted value for the distortion level which determines the full linear response limitation, but we use 3% as a maximum acceptable limit. One subtle point here is that in many applications the distortion which is caused by exceeding the full linear response can be comfortably ignored. But a far more serious effect, often overlooked, is that a DC offset voltage can be generated when the full linear response is exceeded. This is due to rectification of the asymmetrical feedback waveform or overloading the input stage with large distortion signals at the summing junction.

Certain amplifiers designed to optimize high-frequency performance will provide full output swing substantially beyond the full linear response (3% distortion) limit described above. Since linear waveshape is not generally a consideration in the use of these devices, they are specified for the maximum frequency at which they will produce full output swing. This is termed "full peak response" and is indicated as such on the specification charts by the word "peak" in the row marked "Full Power Response."

### *Initial Bias Current*

Bias current,  $i_b$ , is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common mode voltage). For differential amplifiers, bias current is present at both the negative and positive inputs. All Analog Devices specifications pertain to the worse of the two (not average or mean). For single ended amplifiers, bias current refers to the current at the active input only.

Initial bias current,  $I_b$ , is the bias current at either input measured at +25°C, rated supply voltages and zero common mode voltage. The designation (0, +) or (0, -) indicates that no internal compensation has been used to reduce initial bias current and hence the polarity is always known. The sign indicates the power supply polarity to which an external compensating resistor should be connected to zero the initial bias current. The designation ( $\pm$ ) indicates that internal compensation has been used to reduce initial bias current, and that the residual bias current may be of



either polarity. In general, compensating initial bias current has little effect on the bias-current temperature coefficient. One should note that the bias current of FET amplifiers increases by a factor of 2 for each  $10^{\circ}\text{C}$  rise in temperature.

### *Initial Difference Current*

Difference current,  $i_d$ , is defined as the difference between the bias currents of a differential amplifier. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is about 10% of the bias current at either input, assuming that initial bias current has not been compensated.

### *Input Impedance*

Differential input impedance,  $R_d$ , is defined as the impedance between the two input terminals, measured at  $+25^{\circ}\text{C}$ , assuming that the error voltage  $e_e$  is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor,  $C_d$ , in parallel with  $R_d$ .

Common-mode impedance,  $R_{cm}$ , is defined as the impedance between each input and ground (or power supply common) and is specified at  $+25^{\circ}\text{C}$ . For most circuits, common-mode impedance at the negative input  $R_{cm-}$ , has little significance, except for the capacitance which it adds at the summing junction. However, common-mode impedance on the plus input,  $R_{cm+}$ , sets the upper limit on closed-loop input impedance for the non-inverting configuration. Dynamic impedance can be represented by a capacitor,  $C_{cm}$ , in parallel with  $R_{cm}$ ; it usually ranges from 5 to 25pF on the plus input.

Common-mode impedance is a non-linear function of both temperature and common-mode voltage. For FET-input amplifiers, common mode impedance is reduced by a factor of two for each  $10^{\circ}\text{C}$  temperature rise.

As a function of a common mode voltage,  $R_{cm}$  is defined as average impedance for a common mode voltage change from zero



to  $\pm E_{cm}$ , that is, maximum common mode voltage. Incremental  $R_{cm}$  about some large common mode voltage may be considerably less than the specified average  $R_{cm}$ , especially for FET input amplifiers.

### *Initial Offset Voltage*

Offset voltage,  $e_{os}$ , is defined as the voltage required in series with the input from a zero source impedance to drive the output to zero. Initial offset voltage,  $E_{os}$ , defines the offset voltage at  $+25^{\circ}\text{C}$  and rated supply voltages. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

### *Input Noise*

Input voltage and current noise characteristics can be specified and analyzed very much like offset voltage and bias current characteristics. In fact, drift can be considered to be noise which occurs at very low frequencies. The primary difference in measuring and specifying noise as opposed to DC drift is that bandwidth must be considered. At low frequencies, 100Hz or less,  $1/f$  noise prevails, which means that the noise per root cycle increases inversely with the square root of frequency. At the mid-band frequencies noise per root cycle is constant or "white."

For this reason two noise specifications are given. Low-frequency random noise in a pass band of 0.01 to 1Hz is specified as peak-to-peak with a 6.6 rms uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise in a bandpass of 5Hz to 50kHz is specified as rms.

### *Maximum Common-Mode Voltage*

For differential-input amplifiers, the voltage at both inputs can have values above or below ground potential. Common mode voltage, is defined as the voltage (above or below ground) when both inputs are at the same voltage.  $E_{cm}$  is defined as the maximum peak common mode voltage which will produce less than a 1% error at the output.  $E_{cm}$  establishes the maximum input voltage for the voltage follower connection.



### *Open-Loop Gain*

Open loop gain,  $A$ , is defined as the ratio of a change of output voltage to the error voltage applied between the amplifier inputs to produce the change. Gain is usually specified only at DC ( $A_o$ ), but in many applications the frequency-dependence of gain is also important. For this reason, the typical open-loop gain response is published for each amplifier.

### *Overload Recovery*

Overload recovery defines the time required for the output voltage to recover to the rated output voltage  $E_o$  from a saturated condition. In some amplifiers the overload recovery will increase for large impedances (greater than  $50k\Omega$ ) in the input circuit. Published specifications apply for low impedances and assume that overload recovery is not degraded by stray capacitance in the feedback network. Overload recovery is defined for 50% overdrive.

### *Rated Output*

Rated output voltage is the minimum peak output voltage which can be obtained at rated output current before clipping or excessive non-linearity occurs. Rated output current is the minimum guaranteed value of current supplied at the rated output voltage. Load impedance less than  $E_o/I_o$  can be used but  $E_o$  will decrease, distortion may increase and open loop gain will be reduced. (All models are short-circuit protected to ground.)

### *Settling Time*

Settling time is the time required, after a demand for an output step change (such as a step input to a unity-gain follower), for the output to reach and remain at the final value, within a band of specified magnitude. This period includes an initial delay, a period of "slewing" at maximum speed, a period of recovery during which an overshoot or "ringing" may occur, and final relaxation to within the defined error band (sometimes with a long "tail.") For small error bands, such as 0.01%, settling time is difficult to

measure. One approach, used for measuring converter settling time, is discussed in the chapter "Testing Converters." Other means have been discussed in the literature.\*

### *Slewing Rate*

Slewing rate,  $S$ , usually in volts/ $\mu$ sec, defines the maximum rate of change of output voltage for a large input step change.  $S = 2\pi f_p E_o$

### *Temperature Drift*

Offset voltage, bias current and difference current all change or "drift" from their initial values with temperature. This is by far the most important source of error in most applications. The temperature coefficients of these parameters,  $\Delta e_{os}/\Delta T$ ,  $\Delta i_b/\Delta T$ , and  $\Delta i_d/\Delta T$  are all defined as the average slope over a specified temperature range. In general, however, drift is a non-linear function of temperature and the slopes are greater at the extremes of temperature than around normal (+25°C) ambient which generally means that for small temperature excursions, the specification is conservative.

For example, a rather popular method of specifying this extremely important parameter consists of: a) arithmetically subtracting the measured offset values at the upper and lower temperature extremes and b) dividing this difference by the temperature excursion. This can yield an extremely misleading result, particularly where offset drifts in the same direction at the two extremes. It is obviously possible to have no difference in the two end-point measurements, yet severe slopes may exist between the two as illustrated in Figure 9. In this case the apparent (specified) drift would be zero  $\mu V/^\circ C$ .

Analog Devices employs two methods of drift specification — a "true butterfly" curve characteristic for the high performance/low drift models, and a "modified butterfly" for the lower cost amplifiers. Both overcome the deficiencies described above. A

\*For example, *Analog Dialogue*, Vol. 4, No. 1, "Settling Time of Operational Amplifiers"

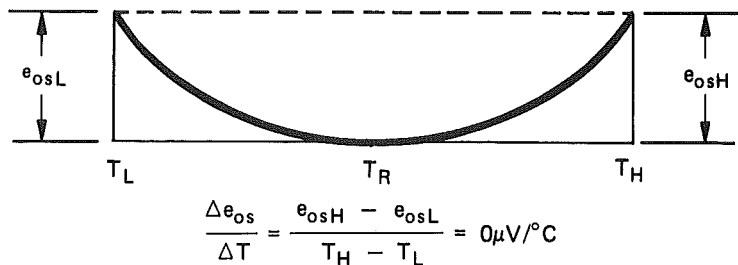


Figure 9. Two-point method of computing Offset Temperature Coefficient

comparison of these methods is shown with definitive equations in Figure 10. Essentially, the butterfly characteristic insures that if the amplifier is adjusted to zero at room temperature ( $T_R$ ), the offset at any temperature would, in no case, exceed the value predicted by multiplying the specified drift rate (in  $\mu V/^{\circ}C$ ) by the temperature excursion.

### BUTTERFLY CHARACTERISTICS

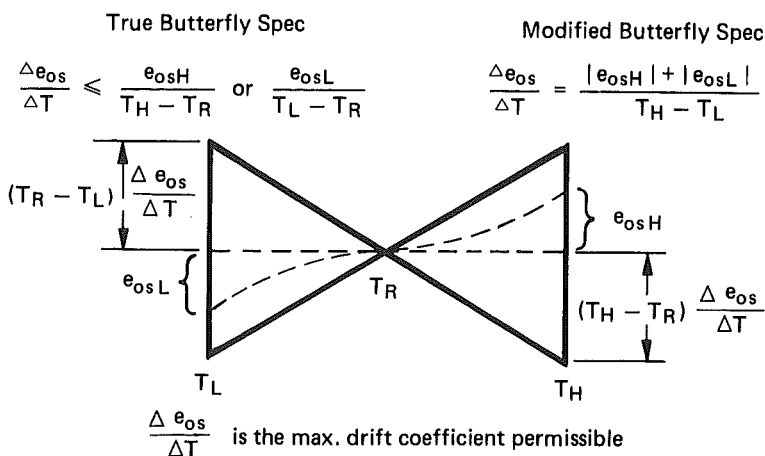


Figure 10. 3-point ("Butterfly") Definition of Offset Temperature Coefficient

### *Unity-Gain Signal Response*

Unity-gain small-signal response,  $f_t$ , is the frequency at which the open loop gain becomes unity or zero dB. "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting or signal rectification. For amplifiers with symmetrical response on both inputs,  $f_t$  may be obtained by either the inverting or non-inverting configurations. Some wideband amplifiers with feed forward design have fast response only on the negative input, which restricts high-speed use to the inverting circuit.

### *SELECTION PRINCIPLES*

In selecting the right device(s) for a specific application, the designer should have clearly in mind the design objectives, a firm understanding of what the published specifications mean, and the significant features affecting the application.

1. *A complete definition of the design objectives* includes signal levels, desired accuracy and bandwidth, circuit impedances, environmental conditions, etc.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Often, two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques,\* creating a pitfall for the designer.

\*An excellent contemporary case in point is the room-temperature bias-current spec for FET-input I.C. op amps. When bias current is measured on automated high-speed test equipment, the chip doesn't have sufficient time to warm up, which means that the reading will be low, often by a factor of 4, because of the doubling per  $10^\circ\text{C}$  temperature rise. At this writing, Analog Devices is one of the few IC manufacturers to take this into account and specify the current actually encountered by the user under equilibrium conditions rather than a useless "test" spec. Also, maximum bias current is specified by Analog Devices as the worse of the two input currents, rather than their average. With the "average" spec, e.g.,  $(0.1 + 1.9)/2 = 1.0$  "Murphy's Law" decrees that the larger current will appear at the active terminal.



### 3. *A checklist of essential characteristics of the design*

A. Character of the application: differential or single-ended, follower or inverter, linear or nonlinear

B. Accurate description of the input signals: voltage or current source, range of amplitudes, source impedance, time/frequency characteristics

C. Environmental conditions: maximum ranges of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment

D. Accuracy desired, as a function of bandwidth, static and dynamic parameters, loading

### *SELECTION PROCESS*

In general, the objective of amplifier selection should be to choose the least-expensive device that will meet the physical, electrical, and environmental requirements imposed by the application. This implies that a “general purpose” amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, the limitations are usually imposed by either bandwidth requirements or offset and drift parameters. As mentioned earlier, an extended discussion of these factors appears in the *Analog Devices Product Guide – 1972* and (if out of print) its successor publications, available upon request.